REMARKS

Attached is a marked-up version of the changes being made by the current amendment.

Applicant asks that all claims be examined. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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Version with markings to show changes made

In the claims:

Claims 1, 9, and 16 have been amended as follows:

1. (Amended) A method comprising:

compressing a plurality of pixel values and a rounding vector into a first sum vector and a first carry vector;

discarding [the] a least significant bit of the first carry vector;

discarding [the] a two least significant bits of the first sum vector; and

adding the first sum vector and the first carry vector to generate a pixel average value.

9. (Amended) Apparatus comprising:

a compressor stage including a plurality of compressors, each compressor operative to compress a plurality of operands and a rounding vector into a first sum vector and a first carry vector and to discard [the] a two least significant bits (LSBs) of said first sum vector and [the] an LSB of the first carry vector; and

a Single-Instruction/Multiple-Data (SIMD) adder operative to add the first sum vector and the first carry vector to generate an average pixel value.

16. (Amended) An article comprising a machine-readable medium include machine readable instructions, the instructions operative to cause a machine to:

compress a plurality of pixel values and a rounding vector into a first sum vector and a first carry vector;

discard [the] a least significant bit of the first carry vector;

discard [the] a two least significant bits of the first sum vector; and

add the first sum vector and the first carry vector to generate a pixel average value.

In the Abstract:

The Abstract has been amended as follows.

In an embodiment, a functional unit including a compressor section and a 36-bit SIMD adder is used to perform a SIMD four-pixel averaging instruction. The functional unit generates four four-pixel averages. Four pixel values and a rounding value are compressed into a sum and a carry vector. The [tow] two least

significant bits of the sum vector and the LSB of the carry vector are dropped before being input to the 36-bit SIMD adder. The two resultant 8-bit vectors are added by the 36-bit adder to directly generate the average pixel value result.